



Sharif University of Technology  
Department of Computer Engineering

# Digital System Design Introduction

Siavash Bayat-Sarmadi

# Syllabus

2

- In general
  - ▣ Verilog hardware description language (HDL)
  - ▣ A glance at FPGAs
  - ▣ ASM charts
  - ▣ Digital design techniques and considerations

# Texts and Refs

3

- Verilog HDL: A Guide to Digital Design and Synthesis, 2nd Edition
  - By: Samir Palnitkar
  
- <http://asic-world.com/>

# Course Content

4

- Intro
- Hierarchical modeling concepts
- Basic concepts
- Module and ports
- Gate level modeling
- Dataflow modeling
- Behavioral modeling
- ASM
- Tasks and functions
- Synthesis
- FSM
- FPGA
- Metastability & CDC
- STA

تمرین	تدریس استاد	تاریخ جلسات درس
-	Introduction, Hierarichal modeling	25 شهریور
-	Basic concepts	27 شهریور
-	Basic concepts	1 مهر
-	Modules and ports, Gate level modeling	3 مهر
-	Gate level modeling	10 مهر
HW1 release Deadline: 21 مهر	Gate level modeling, Modelsim intro.	15 مهر
-	Data flow modeling	17 مهر
HW2 release Deadline: 28 مهر	Data flow modeling	22 مهر
-	Behavioral modeling	24 مهر
-	Behavioral modeling	29 مهر

تمرین	تدریس استاد	تاریخ جلسات درس
-	Behavioral modeling	1آبان
HW3 release Deadline: 12آبان	Behavioral modeling	6آبان
-	ASM	8آبان
-	ASM	13آبان
-	ISE	15آبان
HW4 release Deadline: 3آذر	Tasks and Functions	20آبان
-	Synthesis	22آبان
-	FSM	29آبان
HW5 release Deadline: 10آذر	FPGA	4آذر
-	FPGA	6آذر

تمرین	تدریس استاد	تاریخ جلسات درس
HW6 release Dead line: 17 آذر	Metastability and CDC	11 آذر
-	Metastability and CDC	13 آذر
HW7 release Dead line: 24 آذر	STA	18 آذر
-	STA	20 آذر
-	STA	25 آذر
-	Vivado	27 آذر
HW8 release Dead line: 8 دی	Vivado	2 دی
-	Vivado	4 دی

امتحانات	تاریخ
Midterm Exam	2 آذر
Practical Exam	30 آذر
Final Exam	16 دی

# Evaluation

8

- Midterm Exam: 15% (3 marks)
- Practical Exam: 15% (3 marks)
- Final Exam: 25% (5 marks)
- Assignments & Project: 50% (10 marks)
- Total: 105%(21 marks)



# Tutorials

9

- Head TA:
  - ▣ Mohammad Hossein Farzam (mfarzam@ce)
  
- Course Website
  - ▣ Courseware of SUT (cw.sharif.edu)
  - ▣ Quera (quera.ir)
  
- Tutorial Date/Time/Room (once required)
  - ▣ Sundays/ 12-13:30/ Room 101
  - ▣ Will be held after each HW deadlines

# Evolution of Digital Circuits

10

- Vacuum tubes
- Transistors
- Small Scale Integration (SSI)
- Medium Scale Integration (MSI)
  - ▣ 100s of transistors on a chip
- Large Scale Integration (LSI)
  - ▣ 1000s
- Very Large Scale Integration (VLSI)
  - ▣ 10,000s
  - ▣ Computer-Aided Design (CAD)

# Emergence of HDL

11

- To describe electronic circuits, mainly digital
  - ▣ Design
  - ▣ Simulation
  - ▣ Synthesis

# Verilog HDL

12

- Verifying Logic
- Originated at Automated Integrated Design Systems (later renamed as **Gateway Design Automation**) in 1985
- Designed by Phil Moorby
- IEEE standard 1995
- Syntax based on C programming language

# VHDL

13

- VHSIC HDL: Very High Speed Integrated Circuit Hardware Description Language
- By the U.S Department of Defense
  - to document the behavior of the ASICs
- VHDL 7.2 in 1985
- IEEE standard in 1987
- ANSI standard in 1988
- Syntax based on Ada programming language

# Verilog vs. VHDL

14

## Verilog

- ❑ Designed for hardware design
- ❑ User defined data types are not allowed
- ❑ Low level construct
- ❑ No concept of a library
- ❑ Powerful PLI
- ❑ Case-sensitive
- ❑ More popular in USA

## VHDL

- ❑ Designed for documentation
- ❑ User defined data types are allowed
- ❑ High level construct
- ❑ Library
- ❑ No PLI
- ❑ Not case-sensitive
- ❑ More popular in Europe

# Hello World!!!

15

## Verilog

```
module hello_world;  
initial begin  
$display(  
"Hello World");  
#10 $finish;  
end  
endmodule
```

[www.asic-world.com](http://www.asic-world.com)

## VHDL

```
entity hello_world is  
end;  
architecture  
hello_world of  
hello_world is begin  
stimulus:process  
Begin  
assert flase report  
"Hello World"  
severity note;  
wait;  
end process stimulus;  
end hello_world;
```

# Other HDL example

16

- Digital: ABEL, AHDL, etc.
- Analog: Verilog-AMS, HDL-A, etc.



# Level of Modelling in Verilog

17

- Behavioral level
  - ▣ Functionality
  - ▣ No hardware details
- Dataflow level
  - ▣ How data processed
- Gate level
  - ▣ Wiring between gates
- Switch level
  - ▣ Using transistors



RTL, a mixture of behavioral and dataflow descriptions

# HDL Considerations

18

- Early verification
- Design hierarchy
- Independence of fabrication technology
- Concurrency
- Timing

# VLSI Design Flow

19

